Imaging Quality Full Chip Verification for Yield Improvement

Qing Yang*[a], CongShu Zhou[a], ShyueFong Quek[a], Mark Lu[a], YeeMei Foong[a];

JianHong Qiu[b], Taksh Pandey[b]; Russell Dover[b]

[a]GLOBALFOUNDRIES
60 Woodlands Industrial Park D Street 2, Singapore, 738406
[b]ASML Brion Technologies, 4211 Burton DR., Santa Clara, CA, 95054, USA

ABSTRACT

Basic image intensity parameters, like maximum and minimum intensity values (Imin and Imax), image logarithm slope (ILS), normalized image logarithm slope (NILS) and mask error enhancement factor (MEEF) , are well known as indexes of photolithography imaging quality. For full chip verification, hotspot detection is typically based on threshold values for line pinching or bridging. For image intensity parameters it is generally harder to quantify an absolute value to define where the process limit will occur, and at which process stage; lithography, etch or post-CMP. However it is easy to conclude that hot spots captured by image intensity parameters are more susceptible to process variation and very likely to impact yield. In addition these image intensity hot spots can be missed by using resist model verification because the resist model normally is calibrated by the wafer data on a single resist plane and is an empirical model which is trying to fit the resist critical dimension by some mathematic algorithm with combining optical calculation. Also at resolution enhancement technology (RET) development stage, full chip imaging quality check is also a method to qualify RET solution, like Optical Proximity Correct (OPC) performance.

To add full chip verification using image intensity parameters is also not as costly as adding one more resist model simulation. From a foundry yield improvement and cost saving perspective, it is valuable to quantify the imaging quality to find design hot spots to correctly define the inline process control margin.

This paper studies the correlation between image intensity parameters and process weakness or catastrophic hard failures at different process stages. It also demonstrated how OPC solution can improve full chip image intensity parameters. Rigorous 3D resist profile simulation across the full height of the resist stack was also performed to identify a correlation to the image intensity parameter. A methodology of post-OPC full chip verification is proposed for improving OPC quality at RET development stage and for inline process control and yield improvement at production stage.

Keywords: OPC, image intensity, NILS, MEEF, LMC

1. INTRODUCTION

When the tech node accelerates to shrink, for the most complex designs and low k1 process, good resolution enhancement technology (RET) solution and strong Design for manufacturing (DFM) support have become the prerequisites of wafer patterning. When a RET solution is to be developed for a given technology node, it is well known that different processes have their own process weaknesses and sensitivities to different integrated circuit designs. DFM was introduced to integrate the considerations of traditional design and wafer processing. From a foundry's perspective it is challenging to require customers to change their designs to fit the wafer process. Therefore foundries need to deliver robust RET solutions to minimize any process weakness and to maximize the process margin. As part of the RET solution, optical proximity correction (OPC) should be qualified by OPC verification from the beginning.

Optical Microlithography XXVI, edited by Will Conley, Proc. of SPIE Vol. 8683, 868326

As the process constant k1 of the lithography goes down to below 0.3, the lithography process gives the direct impact on the integration robustness to have enough process margins for the production. In this paper we only focus on the study on metal layer of sub-28nm node. Currently for random logic design, the metal layers' minimum pitch is sub-90nm with the sub-45nm line width and sub-45nm space. This sub-45nm dimension is almost the minimum dimension to be resolved with the single exposure in the hyper-NA scanner with the water immersion tool. With this patterning difficulty the resist process is usually optimized to improve the process window margin by using the thinner resist to have the higher contrast which has the side effect in the etch selectivity. As the resist thickness is lower and the resist contract is higher, usually the etch selectivity becomes worse and the thin metal hard mask in the current trench first metal hard mask process can be eroded during this thin metal hard mask etch process even though the trench first metal hard mask (TFMHM) is using the hard mask to etch the low-k material. In addition this eroded hard mark in the previous etch step can be etched into the low-k material to define the metal space for the metal line insulation during the etching process of the low-k material. The main factors, which will carry the quality of lithography process to the proceeding modules of integration flow like Etch and CMP process, are the photo resist's height and the resist slope after development. The sub-28nm patterning with the single exposure is almost on the edge with the 193nm immersion lithography. The smaller lithography CD makes the aerial image contrast worse, which means higher DC level in the unexposed area. This higher DC level, latent image, can sacrifice the resist thickness in the unexposed area and this recessed resist thickness is very harmful for the etch process with the current hard mask which may induce the metal line bridge. Basic image intensity parameters, like maximum and minimum intensity values (Imin and Imax), image logarithm slope (ILS), normalized image logarithm slope (NILS) and mask error enhancement factor (MEEF) , are well known as indexes of photolithography imaging quality. Imaging quality is more directly related to resist formation quality after exposure, and can physically predict resist profile after development. Image intensity parameters can well perform the full chip verification of resist formation quality.

OPC correction affects the full chip imaging quality and image quality based hot spots will result in pattern based failure at given process conditions. Image quality hot spots are very susceptible to process variables, mainly related to the pattern intensity distribution of local layouts, which may cause bad feature profiles, susceptibility to mask variations or dose variations. For some of these, the local OPC can be modified to give better imaging quality. Some cases will ultimately result in a request for a design change. In this situation a solution needs to be provided to the customer for them to change the layout or the entire RET solution might need to be modified to achieve a global improvement to the image quality (such as a change in source or a different OPC technique). Using image quality parameters to verify the full chip imaging quality through the process window is an effective methodology to verify post-OPC quality.

At production stage, full chip imaging quality verification can capture unique hot spots for different customer's design, which are more fundamental and representative of the process. With these hot spots, it's better for inline to control the real process margin and yield monitoring. For yield improvement point of view, based on the verification result to identify possible layout modification solutions for customer is also valuable, so called DFM solution.

2. METHODOLOGY AND RESULT

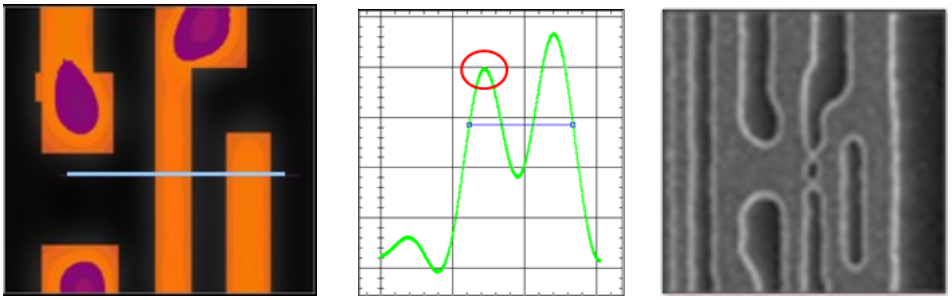
Image quality verification has a number of parameters that can be checked, like maximum and minimum intensity, ILS, NILS and MEEF. Each represents different characteristics of the imaging process. This paper demonstrates the usage of each of these parameters for hot spot detection and control in below part. Wafer data of hot spots are well correlated to the detection value as well.

1. Imin and Imax

The objective of OPC is to achieve full chip imaging that matches the target within a threshold specification. A good OPC solution needs to not only meet the specified critical dimension or edge placement target but also control the image intensity maximum and minimum value of each edge to avoid over or under corrected layouts. When a relative maximum or minimum intensity exceeds the over or under dose threshold unexpected printing results will occur. So for OPC development the full chip image intensity verification defined by Imin and Imax is very

important. Too many Imax or Imin hot spots identifies if the OPC solution is vulnerable to printing problems. For localized critical designs which are sensitive to local OPC movement, the OPC tuning can be directed by image intensity verification.

We take 28nm metal as the case to demonstrate how to use Imax and Imin full chip detection to develop and choose OPC solution in development stage. We use some test layouts and set up Imin and Imax detector and threshold to captures hot spots to verify the hypothesis on the wafer. We show here two examples. Case 1, as shown in Figure1, is the example with a locally lowest Imax value comparing to other locations. We prepared post development and post etch wafer to look into this location. We found the scum can be seen near the wafer bottom but it did not cause the hard failure on post development wafer. But on post etch wafer, obvious trench open appeared which was directly related with the footing resist profile.

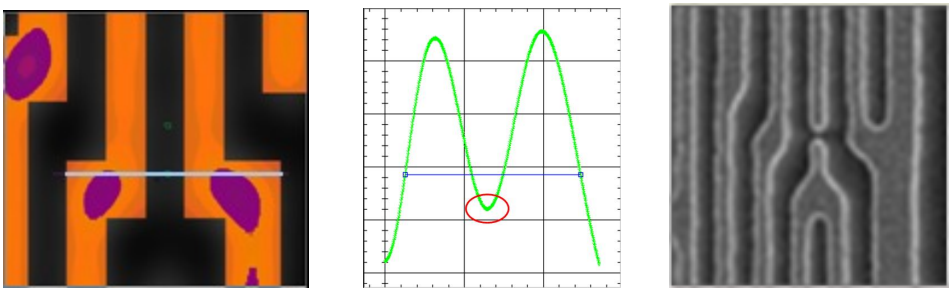


a) b) c)

Figure 1. shows an example where a low Imax value indicates that the trench CD of metal will be undersized and cause post etch open failure.

a) Aerial image simulated intensity through the cut-line for hot spot pattern
b) Intensity curve distribution thru the cut-line shows a locally lowest Imax peak comparing to other Imax values on main feature
c) Post etch wafer shows open of metal trench at the hot spot

Case 2, as shown in Figure2, is the example with a locally highest Imin value comparing to other locations. We also could not find hard bridge or pinch on post development wafer except severe resist top loss was suspected. We proved it on post etch wafer by capturing the hard short of metal line. Resist thickness in this location had degraded to so thin and resist slop has become so steep that the etch profile transferred from resist profile bridged on the top.



a) b) c)

Figure 2. shows an example where a high Imin value indicates that the line CD of metal will be pinched and cause post etch short failure.

a) Aerial image simulated intensity through the cut-line for hot spot pattern
b) Intensity curve distribution thru the cut-line shows a locally highest Imin valley comparing to other Imin values on main feature
c) Post etch wafer shows short of metal line at the hot spot

We confirmed on wafer that Imax and Imin for main features on metal layer are directly correlated to wafer failure. Additionally we can use this methodology for sub-resolution assist feature (SRAF) or side lobe printing margin check. For example, on metal layers, SRAF printing pattern has high Imax value as shown in Figure 3. The Imax value is so close to nominal printing threshold that within production controllable margin it can induce unexpected

printing result, like resist residue inside metal trench. Same hot spot detected by high Imin value shown in Figure 4. With the higher exposure latitude, the positive SRAF of metal layer can resolve with Imin lower than exposure threshold, which will cause unexpected hole printing in blank design area.

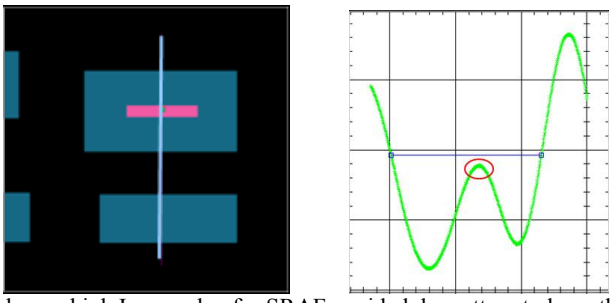


Figure 3. shows an example where a high Imax value for SRAF or side lobe pattern to have the risk to print out.

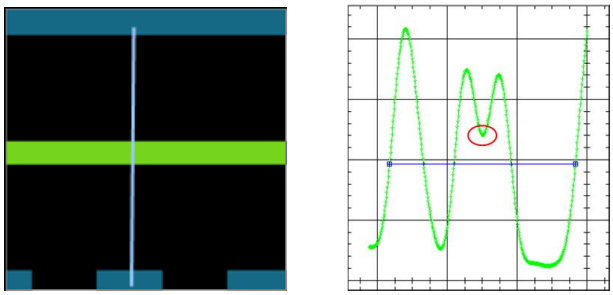


Figure 4. shows an example where a low Imin value for SRAF or side lobe pattern to have the risk to print out.

With full chip detection of Imax and Imin, we can have one more criteria to judge on OPC solutions. Most of the criteria used for OPC migration, are the convergence of EPE distribution of full chip. But as the process and design come to such challengeable level, the request for OPC is not only nominal and process window CD contour to meet the spec, but also the OPC solution can provide as big as much process margin for process variation. Full chip Imin and Imax value distribution was such an index to let us know the OPC robustness on potential hot spots in optics. As shown in Figure 5, OPC2 gave less Imin and Imax hot spots with better simulation value at worst case. With comparable convergence results of full chip EPE distribution, OPC2 is the better solution for this case.

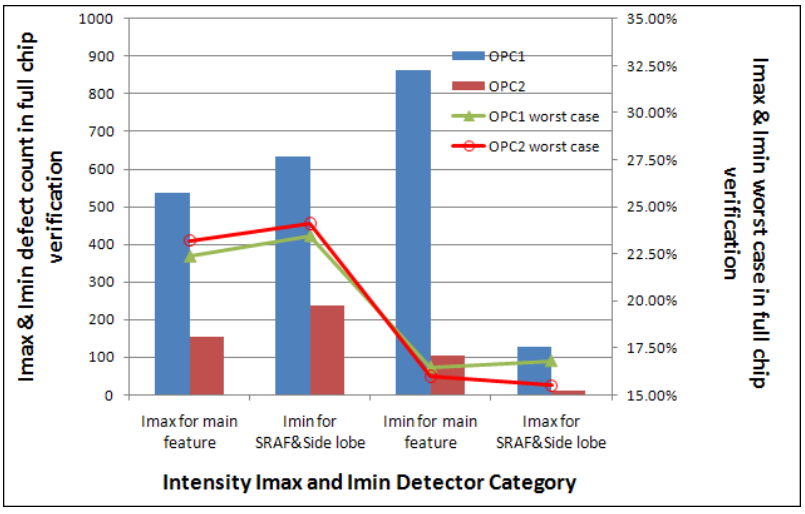
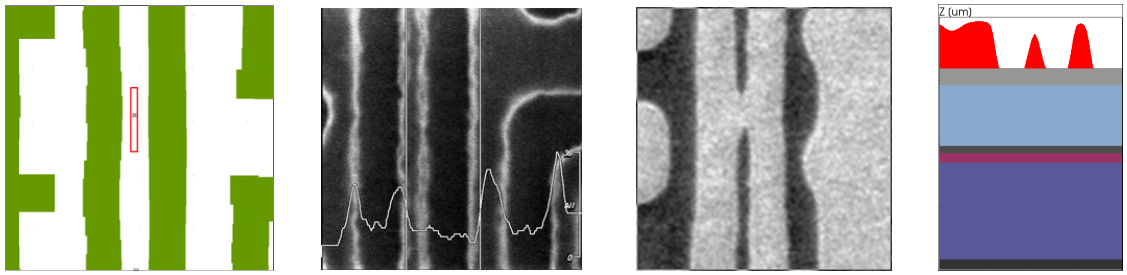


Figure 5. Different OPC solutions show different Imin and Imax distribution on full chip, which can be used as one of criteria to choose final OPC solution.

2. Normalized image log slope (NILS)

NILS checks are more focused on imaging contrast, which is an important index for resist printing quality. In general NILS values are dominated by optical characteristics, including the localized layout of the design. Historically NILS has been correlated to the resist CD as measured at the bottom of the resist stack. Current studies however have shown a correlation between NILS hotspots and hotspots due to poor resist profile which can result in catastrophic failure after etch and CMP. The example shown here in Figure 6 identifies a NILS based hotspot where complete pattern failure is seen at CMP, despite the bottom resist CD after lithography being simply marginal, rather than catastrophic. Figure 4 shows another NILS hotspot location where rigorous simulation was also performed to look at the 3 dimensional resist profile which identified significant resist top loss. Without understanding that the NILS value has this correlation to resist failure this hotspot might have simply been flagged for local OPC modification when in fact a more significant improvement is required such as a layout revision, a change in RET used, or an improvement in the resist process.



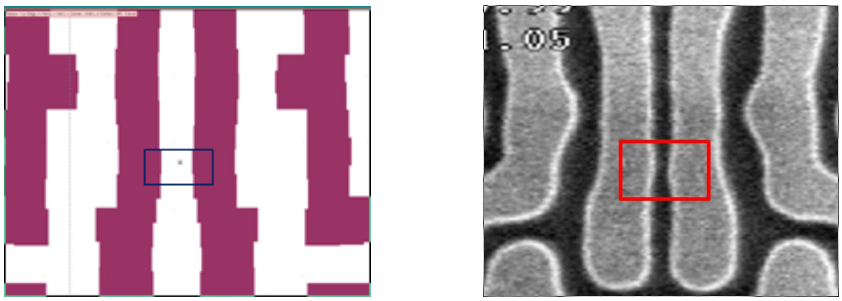
a) b) c) d)

Figure 6.NILS hot spot detected in full chip verification.

a) Hot spot and error marker
b) Litho wafer profile shows steep resist slop at the hot spot location
c) Post CMP wafer shows short of metal line at the hot spot
d) With rigorous simulation tool, the steep resist profile can be proven at the location

3. Mask error enhancement factor (MEEF)

MEEF is a key factor for the quality of OPC solution. Thus process window OPC (PWOPC) needs to include mask bias in its optimization and not simple focus and dose (or just nominal condition optimization). Figure 1 shows an example where at layout the nominal condition post OPC layout performed without mask bias in its optimization does not show as a hotspot, however the wafer results shows a mask error based hotspots.



a) b)

Figure 7.MEEF hot spot detected in full chip verification.

a) Post OPC layout without mask bias included in the optimization. Captured as MEEF hot spot by image check
b) Wafer result shows fidelity of MEEF check

But in PWOPC, several process conditions are combined together and competing each other so that the weight and condition variation setting become very critical. In general, MEEF detection in full chip is still an aspect to validate a PWOPC solution.

3. CONCLUSION

To qualify a RET solution, especially the OPC recipe, full chip verification using image quality metrics, and not just critical dimension or edge placement based criteria, becomes essential. Using image quality parameters to verify the full chip imaging quality through the process window is an effective methodology to verify post-OPC quality. It is fundamentally different from conventional verification flow by using calibrated resist model, which is contour based and half empirical. Imaging quality is closer to physical nature of printing process and more related to proceeding integrated module flow, like etch and CMP. So imaging quality verification in full chip is a good methodology for capturing the hot spots impacting yield and reliability at production stage as well.

4. FUTURE WORK

In the future, we will focus on explore correlation between imaging quality in single layer and process integration between interconnect layers. The relationships between these image intensity parameters are also the key to separate different optical effects and study the source of the limit in current PWOPC solver.

REFERENCES

[1] Hye-Young Kang, et al, "Mask error enhancement factor variation with pattern density", Proc. SPIE 5992 (2005).
[2] Ulrich Klostermann, "Calibration of physical resist models: methods, usability, and predictive power," J.Micro/Nanolith.MEMS MOEMS 8, 033005 (2009).
[3] Bong-Soo Kang, et al, "Model-based searching method to find the integrated critical failure on the wafer", SPIE Vol. 8327 (2012).